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Full Length Research Paper

A Novel Design of Multilevel Inverter Topology with Reduced Switch Count

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Abstract
At present multilevel converters are technically interesting due to their high-power handling capabilities, low output harmonics level. The multilevel inverters configurations now in use have as their main disadvantage their circuit complexity, requiring a great number of power devices and passive components in their implementation, and increasing control circuit complexity. Which leads to system cost is rather high, and therefore the multilevel inverters are considered cost effective only in very high-power applications. In this paper, a novel design of multilevel inverter having a reduced switch count is presented, based upon the H-Bridge with auxiliary switch architecture. This novel design configuration is implemented with a new microcontroller based PWM controller is introduced. The combination of the new multi-level inverter topology and the new microcontroller based controller circuit reduces both system cost and complexity. This novel design is validated through PSIM simulation software and compared with the conventional cascaded H-bridge inverter the comparative results shows that the novel topology works properly to generate multilevel voltage waveform with comparatively improved efficiency and low switching losses. The hardware was implemented and tested and it found results are very close to the simulation results.

Key Words: *Multilevel inverter topology's, H-Bridge inverter, Microcontroller based PWM.*

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Introduction

The multilevel voltage source inverters unique structure allows them to reach high voltages with low harmonics without use of transformers or series connected synchronized switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from dc voltages. For this reason multilevel inverters can easily provide the high power required of a large electric drives. As the number increases the synchronized output waveform has more steps, which produces a staircase waveform that approaches a desired waveform. Also as more steps are added to the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels increases. Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system.

Number of multilevel converter topologies has been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. Moreover, three different major multilevel converter structures have been discussed in this paper: cascaded H-bridges converter with separate dc sources is illustrated in Figure 1. It consists of a series of H-bridge inverter units separate dc source is connected to each H-bridge inverter. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. However, the requirement of isolated dc voltage source, a large number of power switching devices and their gate drive circuits are fatal drawback brought by this configuration. Another topology proposed here is diode clamped inverter is shown in figure 2. Each active switching device is required to block only a voltage level of V_{dc}, the clamping diodes require different ratings for reverse voltage blocking is the major disadvantage of this configuration. The number of diodes required for each phase would be (m-1) × (m-2) which is the added losses. And flying capacitors (capacitor clamped) The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping

diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Figure 3. In addition to the (m-1) dc link capacitors, the m-level flying-capacitor multilevel inverter will require (m-1) × (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. Control is complicated to track the voltage levels for all of the capacitors. Also, pre-charging all of the capacitors to the same voltage level and startup are complex. The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Table I present the Comparison of three different multilevel level Inverters and number of component required to implement a nine-level inverter using three defined ones.

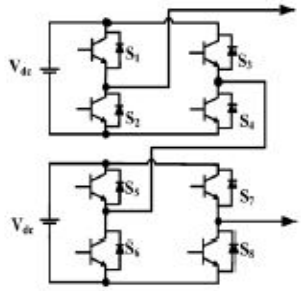

Fig 1. Cascaded H-Bridge Multilevel Inverter.

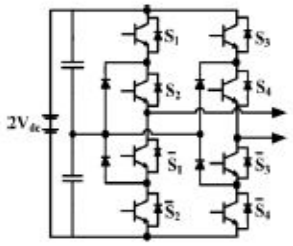

Fig 2. Diode Clamped Multilevel Inverter.

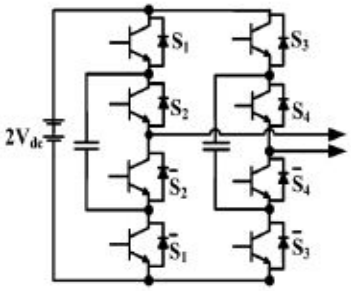

Fig 3. Flying Capacitor Multilevel Inverter.

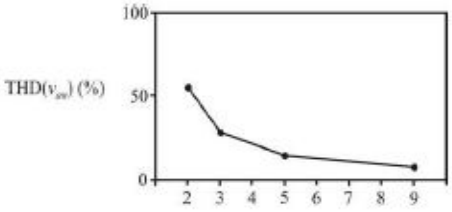

Fig 4. Graph between THD in % and Number of inverter level

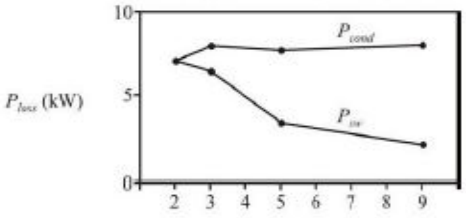

Fig 5. Graph between Power loss in KW and Number of inverter level

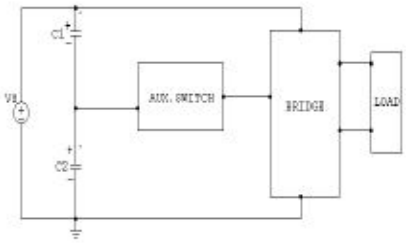

Fig 6. Block diagram H-Bridge with auxiliaryswitch Multilevel inverter

Problem identified

The multilevel converter configurations shown above have their disadvantages are identified as. If the number of levels is increased to reduce the THD simultaneously the power losses is increased due to greater number of switches. Requiring a great number of power devices and passive components in their implementation also Increasing control circuit & Isolation circuit complexity. A system cost is rather high and therefore the multilevel inverters are considered cost effective only in very high power applications. The figure 4 & 5 shows the graph between the reduced THD with increased number of level and power lose with increased number of level respectively. We also find three disadvantages of in increased number of levels are: Increased power loss, complicate control flow, increased manufacturing costs. We can consider four important categories to reduce losses in inverters: switching techniques such as soft switching resonant circuits can achieve both the benefits of switch transition control and switching loss reduction, Using the passive snubber reduces switching losses by limiting the active switches di/dt and dv/dt during switching transition with the help of passive devises, Active gate driver based di/dt and dv/dt control technique the gate-controlled di/dt and dv/dt approach looks very attractive since a very compact design could be achieved without adding extra components in the power circuits and Reducing the number of

electronic devices can improve the three following points: reduced switching losses, reduced complicated control and improved manufacturing costs.

Table 1. Comparison of Three Different Multilevel Level Inverters.

Type of multilevel inverter & Required devices	Cascaded H-Bridge multi level inverter	Diode clamped multi level inverter	Capacitor clamped multi level inverter
Main controlled switches	2(M-1) 16	2(M-1) 16	2(M-1) 16
D.C voltage source	(M-1)/2 4	1	1
Diodes	16	((M-1)(M-2)) 56	16
Capacitors	4	(M-1) 8	(M-1)+(M-1)x(M-2)/2 36

Proposed H-bridge with Auxiliary Switch Inverter Circuit Configuration and Principle Operation

The different multilevel inverter topologies presented above are associated with main disadvantage of their circuit complexity, requiring a high number of power switches. Hence we are entering to the new converter topology it includes an H-Bridge stage, with an auxiliary bidirectional switch. This new configuration reduces number of electronic components as power switch count, gate driver circuit which reduces circuit complexity and cost. The block diagram is presented in Fig 6. The modulator and firing control circuit developed using a microcontroller (89C51). Using these two concepts the nine-level H-Bridge with auxiliary switch inverter is presented below.

A. Circuit Configuration

The new converter topology used in the power stage offers a reduced power switch component count and reduced circuit complexity, when compared with the conventional converters presented above. Table II present the number of component required to implement a nine-level inverter using simplified H- bridge multilevel inverter and three previously defined ones: the two that considered as the standard multi-level stages, the diode clamped and the capacitor clamped configuration, and a new and highly improved multi-level stage, the symmetric cascade configuration. The microcontroller based modulator circuit performs all required modulation which is an added advantage in reduced cost and circuit complexity.

Table 2: Comparison of Different Multilevel Level Inverters with Proposed H-Bridge Auxiliary Switch Inverter

Multilevel inverter type	H-Bridge auxiliary switch	Diode clamped	Flying capacitor	Cascaded type
Main controlled switches	4	16	16	16
Auxiliary controlled switches	3	0	0	0
Diodes	16	56	16	16
Capacitor	4	8	36	4

B. Operation Principle of Inverter Circuit

The simplified nine-level H- bridge inverter is presented in Fig 7. The H-bridge is formed by four main power devices, S_1 to S_4. For nine level output voltage, three auxiliary switches, four main switches and four capacitors requires. This new topology achieves a around 40% reduction in the number of main switches required, using only seven controlled power switches instead of sixteen required in any of the other three configurations. The auxiliary switch voltage and current rating are lower than the once required by the main controlled switches. And the reduced number of diodes and capacitors, when compared with diode clamped configuration and capacitor clamped configuration. The new configuration uses no more diodes or capacitors that the second best topology in the table, the asymmetric cascade configuration. Since four capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multi-level configuration.

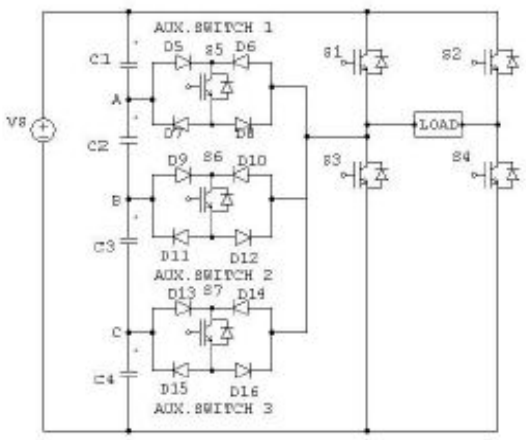

Fig 7. Nine-level H-Bridge with auxiliary switch multilevel inverter

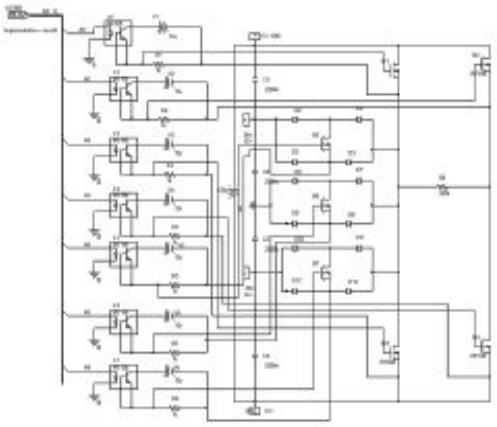

Fig .8 Simulated Circuit of Nine-Level Cascaded Multilevel Inverter

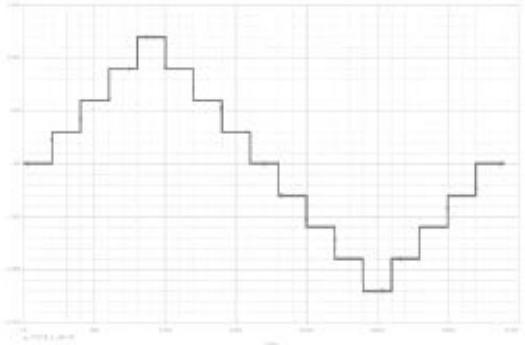

Fig .9 Simulated Nine-Level Output Voltage

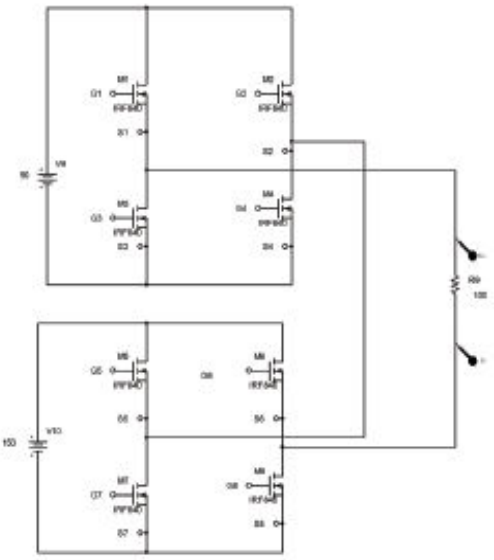

Fig.10 Simulated Circuit of Nine-Level Cascaded

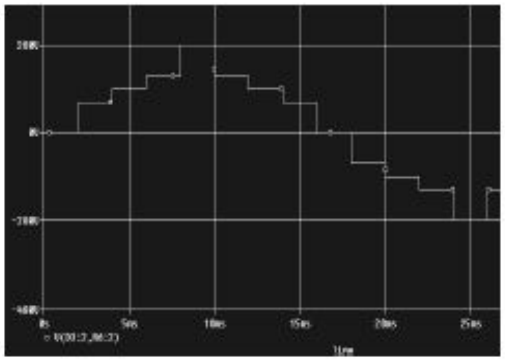

Fig.11 Simulated Nine-Level Output Voltage

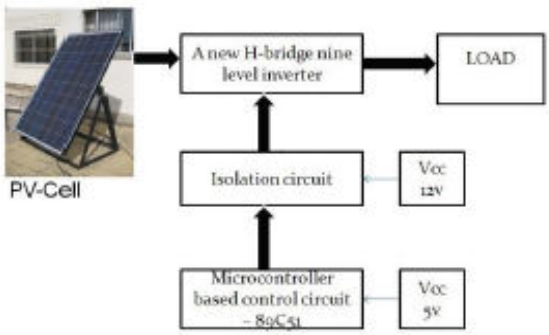

Fig.12 Block Diagram of Nine-Level Inverter.

The switching state combinations required to generate nine-level voltage waveform is shown in TABLE III. The required nine-level output voltage levels (Vs, 3Vs/4, Vs/2, Vs/4, 0, -Vs/4, -Vs/2,-3Vs/4, -Vs) are generated as follows:

a) Positive output level (Vs): S_1 is ON, connecting the load to positive terminal of Vs and S_4 is on, connecting the load to negative terminal of Vs. All other control switches are OFF. The voltage applied to load terminals is Vs

b) Positive output level (3Vs/4): The auxiliary switch S_5 is ON, Connecting the load to positive terminal of Vs, through diodes D_5 and D_8, and S_4 is ON, connecting the load to negative terminal of Vs. All other control switches are OFF; the three capacitor voltage sources are summed up and applied to load terminals is 3Vs/4.

c) Positive output level (Vs/2): The auxiliary switch S_6 is ON, connecting the load to positive terminal of Vs, through diodes D_9 and D_{12} and S_4 is ON, connecting the load to negative terminal of Vs. All other control switches are OFF; the two capacitor voltage sources are summed up and applied to the load terminals is Vs/2.

d) Positive output level (Vs/4): The auxiliary switch S_7 is ON, connecting the load to positive terminal of Vs, through diodes D_{13} and D_{16} and S_4 is ON, connecting the load to negative terminal of Vs. All other control switches are OFF; the single capacitor voltage source is applied to the load terminals is Vs/4.

e) Zero output level: The two main switches S_3 and S_4 are ON, short circuiting the load. All other control switches are OFF; the voltage applied to the load terminals is zero.

f) Negative output level(-Vs/4): the auxiliary switch S_5 is ON, connecting the load to negative terminal of Vs, through diodes D6 and D7 and S2 is ON, connecting the load to positive terminal of Vs. All other control switches are OFF, the single capacitor voltage source is applied to the load terminals is –Vs/4.

g) Negative output level(-Vs/2): the auxiliary switch S_6 is ON, connecting the load to negative terminal of Vs, through diodes D10 and D11 and S2 is ON, connecting the load to positive terminal of Vs. All other control switches are OFF, the two capacitor voltage are summed up and applied to load terminals is –Vs/2.

h) Negative output level (-3Vs/4): The auxiliary switch S_7 is ON, connecting the load to negative terminal of Vs, through diodes D14, D15 and S2 is ON, connecting the load to positive terminal of Vs. All other control switches are OFF, the three capacitor voltage source are summed up and applied to load terminals is -3Vs/4.

i) Negative output level (-Vs): S2 is ON, connecting the load to positive terminal of Vs and S3 is ON, connecting the load to negative terminal of Vs. All other control switches are OFF, the voltage applied to the load terminals is –Vs.

Table 3. Switching Combinations Required to Generate Nine- Level Output Voltage Waveform

S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_{RL}
1	0	0	1	0	0	0	V_S
0	0	0	1	1	0	0	$3V_S/4$
0	0	0	1	0	1	0	$V_S/2$
0	0	0	1	0	0	1	$V_S/4$
0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	$-V_S/4$
0	1	0	0	0	1	0	$-V_S/2$
0	1	0	0	0	0	1	$-3V_S/4$
0	1	1	0	0	0	0	$-V_S$

Computer Simulation.

In order to test the proper operation of the proposed H-Bridge with auxiliary switch multilevel inverter topology, the simplified nine-level H- bridge inverter is presented in Fig 5 are tested by using computer simulations with a PSIM software. The test parameters are listed in TABLE IV. Also in order to compare the proposed topology with the conventional multilevel inverter, the conventional cascaded nine level inverter is simulated using PSIM software. The test parameters are listed in TABLE V. Figure.8 Shows that simulated circuit of Nine-level H-Bridge multilevel inverter. Fig.9 shows that simulated nine-level output voltage waveform. It is clearly visible that the simulated ouput is very close to ideal output defined for nine-level inverter. Fundamental frequency is 50 Hz. It can be seen that the pulse duration is variable depending on the modulator previous state. The nine voltage levels in the figure are Vs = 120V, 3Vs/4 = 90V, Vs/2 = 60V, Vs/4 = 30V, 0V, -Vs/4 = -30V, -Vs/2 = -60V, -3Vs/4 = -90V, --Vs = -120V.

Hardware Circuit Design

Experimental validation of the H-bridge Nine level inverter is going to achieve by using the configuration shown as Fig.5. Four main blocks are going to present: Microcontroller based PWM control block, the driver circuit, PV-Cell voltage source and the nine-level inverter power stages as shown in Fig.10.

A. Microcontroller Based Control Circuit.

The control circuit generates the control signal for all the power components in the power stage on nine-level inverter. In this implementation, the programmable microcontroller based (89C51) PWM control are used. All programs are going to done in assembly language.

Table 4. Test Parameters of nine level H- Bridge inverter

Vs (input voltage source)	120V
Capacitor (C1, C2, C3&C4)	2200microF
Load resistance (RL)	500 K ohms
MOSFET (M1-M7)	IRF840
Output voltage levels	+120, + 90, +60, +30, 0, -30, -60, -90, -120 volts

Table 5. Test Parameters of nine level cascaded inverter

Vs (input voltage source)	$150V_1$, $50V_2$
Load resistance (RL)	1000 K ohms
MOSFET (M1-M8)	IRF840
Output voltage levels	+200, + 150, +100, +50, 0, -50, -100, -150, -200 volts

B. Isolation Circuit.

The isolation circuit will provide the required isolation and power gain between the control circuit and power devices gate.

C. PV-Cell Voltage Source.

The photovoltaic cell is used as the input voltage source for the inverter power stage. However, solar and wind energy systems make use of advanced power electronics technologies and, therefore the in this paper the solar photovoltaic is utilized.

D. Power Circuit.

The power circuit has been assembled by using MOSFET H-bridge with auxiliary switch module. The auxiliary switch is containing diodes and MOSFET.

Table 6. Hardware Parameters of nine level H- Bridge inverter

Vs (input voltage source)	15V
Capacitor (C1, C2, C3&C4)	220 microF
Load resistance (RL)	10 K ohms
MOSFET (M1-M7)	IRF840
Output voltage levels	+15, + 11.25, +7.5, +3.75, 0, -3.75, -7.5, -11.25, -12 volts

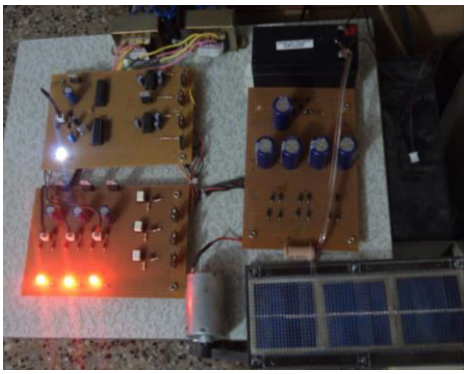

Fig.13 Hardware Image of Nine-Level

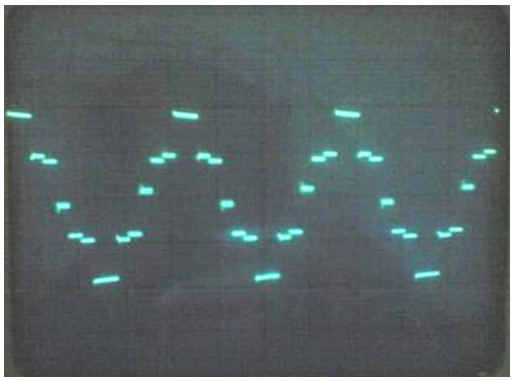

Fig.14. CRO output Image of Nine-Level

Results

The performance of proposed inverter reduced total power loss is verified using efficiency improved factor (EIF)which is given as, EIF= η1- η2 / η2

Where, η1 and η2 are the efficiencies of proposed inverter with reduced number of switch count and conventional cascaded inverter respectively.

The total inverter power loss is calculated by taking following parameters into account

(a) Switching Losses

Switching losses depends on switching frequency of devices. Switching frequency *fs = 1/Ts* where *Ts* is the switching period. Switching losses become dominant part of the total power loss in high switching frequency applications.

(b) Conduction Losses

p = ic Von [*ic* – on state current; *von* – on-sate saturation voltage] Conduction losses are proportional to magnitude of load current.

(c) Off-state Losses

Off-state losses are insignificant for normal ambient temperature.

Comparison of simulated results: Conventional nine-level inverter:

Total input power = 101.35Watts
Total output power = 81.05Watts.
Total power loss = 20.3 Watts
Efficiency η2 = 0.799

Simplified H-Bridge nine-level inverter:

Total input power = 132 Watts
Total output power = 116.7 Watts.
Total power loss = 15.3 Watts
Efficiency η1 = 0.869

Efficiency improvement factor

EIF= η1- η2 / η2 = 0.0876

Hardware results:

Total input power = 560 mWatts
Total output power = 455 mWatts.
Total power loss = 105 mWatts
Efficiency η1 = 0.812

Table 7. Comparison of conventional & proposed nine level inverter simulation results and comparison of Hardware results & simulated results of proposed nine level inverters

Parameters	Proposed H-bridge nine level inverter		Conventional cascaded nine-level inverter
	Simulation results	Hardware results	Simulation results
Voltage in Volts	240 v	15v	150v, 50v
Input power in watts	132 w	560mw	101 .35w
Output power in watts	116.7 w	455mw	81.05 w
Efficiency %	86.9%	81.25%	79.9%

Conclusion

The study of different types of multilevel inverter topologies are compared with their required power devices and passive components. From which the reduced switch count for nine-level is derived from the basic H-bridge inverter with auxiliary switch architecture. This novel design of multilevel inverter with seven switches for nine-level is simulated in computer using PSIM simulation software. From the computer simulation results show that the novel design of proposed circuit has a 3% of reduced switching power loss compared with the conventional nine-level inverter. The (EIF) Efficiency Improvement Factor 8.76%. And this feature makes it more advantages for low& medium power applications with reduced power loss, improved efficiency, less cost and reduced circuit complexity.

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